

PATENT

AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1-33. (Canceled)

34. (Previously presented) An integrated circuit comprising a memory array having at least two planes of memory cells formed above a substrate, said memory cells comprising thin film modifiable conductance switch devices and which cells are arranged in a plurality of series-connected NAND strings, said memory array comprising a first plurality of zias, each of said first plurality of zias respectively coupling a first end of a respective NAND string on each of two or more memory planes to a respective global bit line, and said memory array further comprising a second plurality of zias, each of said second plurality of zias respectively coupling a second end of a respective NAND string on each of two or more memory planes to an associated bias node.

35. (Canceled)

36. (Original) The integrated circuit of claim 34 wherein said switch devices include a charge storage dielectric.

37. (Original) The integrated circuit of claim 36 wherein said charge storage dielectric comprises an oxide-nitride-oxide dielectric stack.

38. (Original) The integrated circuit of claim 34 wherein said switch devices include a floating gate electrode.

39. (Previously presented) The integrated circuit of claim 34 wherein adjacent NAND strings are respectively coupled to a respective global bit line by way of a respective zia structure having a pitch matching that of the NAND strings.

40. (Original) The integrated circuit of claim 34 further comprising NAND strings including a series select device at each end thereof.

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41. (Canceled)

42. (Previously presented) The integrated circuit of claim 34 wherein the substrate comprises a monocrystalline substrate including circuitry which is coupled to the memory array.

43. (Previously presented) The integrated circuit of claim 34 wherein the substrate comprises a polycrystalline substrate.

44. (Previously presented) The integrated circuit of claim 34 wherein the substrate comprises an insulating substrate.

45. (Original) The integrated circuit of claim 34 wherein the thin film modifiable conductance switch devices comprise silicon nanoparticles.

46. (Original) The integrated circuit of claim 34 wherein the thin film modifiable conductance switch devices comprise a polarizable material.

47. (Original) The integrated circuit of claim 34 wherein the thin film modifiable conductance switch devices comprise a ferroelectric material.

48. (Original) The integrated circuit of claim 34 wherein the thin film modifiable conductance switch devices comprise transistors having a depletion mode threshold voltage for at least one of two data states.

49. (Original) The integrated circuit of claim 34 embodied in computer readable descriptive form suitable for design, test, or fabrication of the integrated circuit.

50-52. (Canceled)

53. (Currently amended) The integrated circuit of claim 34 ~~claim 52~~ wherein: adjacent NAND strings share a single zia coupled to an associated bias node.

54-55. (Canceled)